IN THE CLAIMS

Please amend the claims as follows:

1. (Previously Presented) A radio-frequency identification (RFID) circuit for use within an RFID tag, the circuit including:

first clock generation circuitry to generate a modulator clock signal using a first oscillator within the RFID circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory associated with the RFID tag; and

second clock generation circuitry to generate a demodulator clock signal using a second oscillator within the RFID circuit, the demodulator clock signal being recovered from a radio-frequency signal received at the RFID tag.

2. (Previously Presented) The circuit of claim 1, wherein the second clock generation circuitry is to recover a clock signal from the radio-frequency signal received at the RFID tag, to compare the recovered clock signal to an oscillator clock signal generated by the second oscillator and to store a second calibration value, based on the difference between the recovered clock signal and the oscillator clock signal, within a memory device associated with the RFID circuit.

3. (Previously Presented) The circuit of claim 2, wherein the second clock generation circuitry includes calibration circuitry to calibrate the second oscillator utilizing the second calibration value.

4. (Original) The circuit of claim 2, wherein the second calibration value is stored within a volatile memory associated with the RFID tag.

5. (Previously Presented) The circuit of claim 1, wherein the first clock generation circuitry is to retrieve the first calibration value from the non-volatile memory associated with the RFID tag, and to generate the modulator clock signal by calibrating the first oscillator utilizing the first calibration value.

6. (Original) The circuit of claim 1, wherein the first clock generation circuitry is to generate a system clock signal based on the first calibration value stored within the non-volatile memory associated with the RFID tag.

7. (Previously Presented) A method of generating a demodulator clock signal and a modulator clock signal within a radio-frequency identification (RFID) circuit for use within an RFID tag, the method including:

generating the modulator clock signal utilizing a first oscillator included in the RFID circuit and a first calibration value stored within a non-volatile memory associated with the RFID tag; and

generating the demodulator clock signal from a radio-frequency signal received at the RFID tag using a second oscillator included in the RFID circuit.

8. (Previously Presented) The method of claim 7, wherein the generating of the demodulator clock signal includes recovering a clock signal from the radio-frequency signal received at the RFID tag, comparing the recovered clock signal to an oscillator clock signal generated by the second oscillator and storing a second calibration value, based on the difference between the recovered clock signal and the oscillator clock signal, within a memory device associated with the RFID tag.

9. (Previously Presented) The method of claim 8, wherein the generating of the demodulator clock signal includes calibrating the second oscillator utilizing the second calibration value.

10. (Original) The method of claim 8, wherein the second calibration value is stored within a volatile memory associated with the RFID tag.

11. (Previously Presented) The method of claim 7, including retrieving the first calibration value from the non-volatile memory associated with the RFID tag, wherein the generating of the modulator clock signal includes calibrating the first oscillator utilizing the first calibration value.

12. (Original) The method of claim 7, including generating a system clock signal based on the first calibration value stored within the non-volatile memory associated with the RFID tag.

13. (Previously Presented) A radio-frequency identification (RFID) circuit for use within an RFID tag, the circuit including:

first means for generating a modulator clock signal using a first oscillator within the RFID circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory associated with the RFID tag; and

second means for generating a demodulator clock signal within the RFID circuit, the demodulator clock signal being recovered from a radio-frequency signal received at the RFID tag using a second oscillator included in the RFID circuit.

14. (Currently Amended) A computer-readable ~~machine-readable~~ medium storing computer executable instructions comprising a behavioral level description of a radio-frequency identification (RFID) circuit for use in an RFID tag, the computer executable instructions ~~behavioral level description~~ including information to cause a simulator to model behavior of the RFID circuit, said RFID circuit comprising:

first clock generation circuitry to generate a modulator clock signal using a first oscillator within the RFID circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory associated with the RFID tag; and

second clock generation circuitry to generate a demodulator clock signal within the RFID circuit, the demodulator clock signal being recovered from a radio-frequency signal received at the RFID tag using a second oscillator included in the RFID circuit.

15. (Canceled)

16. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 14 [[15]], wherein the behavioral level description is compatible with a very high speed integrated circuit (VHSIC) hardware description language (VHDL) format.

17. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 14 [[15]], wherein the behavioral level description is compatible with a Verilog hardware description language format.

18. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 14, wherein the behavioral level description comprises a register transfer level netlist.

19. (Currently Amended) The computer-readable ~~machine-readable~~ medium of claim 14, wherein the behavioral level description comprises a transistor level netlist.

20. (Previously Presented) An apparatus, including:

a radio-frequency identification (RFID) tag; and

a circuit included in the RFID tag, the circuit including a first oscillator and first clock generation circuitry to generate a modulator clock signal within the circuit, the modulator clock signal being generated utilizing a first calibration value stored within a non-volatile memory included in the RFID tag, and second clock generation circuitry to generate a demodulator clock signal within the circuit, the demodulator clock signal being recovered from a radio-frequency signal received at the RFID tag using a second oscillator included in the circuit.

21. (Previously Presented) The circuit of claim 1, wherein the first calibration value serves as a control input to the first oscillator.

22. (Previously Presented) The method of claim 7, further including:

providing the first calibration value for storage in the non-volatile memory using an RFID reader device.

23. (Previously Presented) The method of claim 7, further including:

using a circuit test device to command storage of the first calibration value in the non-volatile memory via one of a wired link and a wireless link.

24. (Previously Presented) The apparatus of claim 20, further including:

a calibration module to recover timing information from a programming signal, and to generate the first calibration value.

25. (Previously Presented) The apparatus of claim 20, further including:

a tag state machine to select one of a plurality of calibration values, including the first calibration value, stored in the non-volatile memory.